Please amend the present application as follows:

Claims

The following is a copy of Applicant's claims that identifies language being added with underlining ("___") and language being deleted with strikethrough ("—"), as is applicable:

1-10. (Canceled)

11. (Currently amended) A system for verifying data in a data storage device, the data storage device storing data in a number of accessible address locations, said system comprising:

means for designating a range of addresses from said number of accessible address locations as addresses to be verified;

means for verifying whether or not data stored in a starting address of said addresses to be verified contains an error;

means for incrementing the verified address;

means for determining whether or not the incremented address is at the end of the range of addresses to be verified;

means for changing the address to the next address when said means for determining has determined that the incremented address is not at the end of the range of addresses to be verified; ~~and~~

means for resetting the address to an address at the start of the range of addresses to be verified when said means for determining has determined that the address is at the end of the range of addresses to be verified such that all addresses within the range can be re-verified in a continuous loop;

means for interrupting the verifying upon detecting an error in data of one of the addresses; and

means for resuming the continuous loop.

12. (Original) The system of claim 11, further comprising means for counting the number of errors detected by said means for verifying.

13. (Original) The system of claim 11, further comprising means for storing output results from said means for verifying.

14. (Currently amended) A computer-readable medium containing computer-readable instructions~~, the comprising~~ which are executable to:

input a starting address and an ending address so as to define a range of addresses to be verified;

verify whether or not data stored at an address in the range contains an error;

determine whether or not the verified address is the ending address; ~~and~~

initiate verification of the first address if the verified address is the ending address such that all addresses within the range can be re-verified in a continuous loop;

interrupt the verifying upon detecting an error in data of one of the addresses; and

resume the continuous loop.

15. (Currently amended) The computer-readable medium of claim 14, wherein verifying comprises repeatedly verifying ~~comprises~~ until an error is detected.

16. (Previously presented) The computer-readable medium of claim 14, further comprising instructions executable to initiate an interrupt upon detection of an error by said logic configured to verify, wherein initiating an interrupt comprises correcting the data detected in the error.

17-18. (Canceled)

19. (Currently amended) A computer-implemented method for verifying data stored in a data storage device, comprising:

sequentially verifying whether or not data stored at multiple addresses within a range of addresses defined by a starting address and an ending address contains an error; ~~and~~

continuously repeating the sequential verifying of the multiple addresses within the range in a continuous loop such that the verifying can continue indefinitely;

interrupting the sequential verifying upon detecting an error in data of one of the multiple addresses; and

resuming the continuous repeating of the sequential verifying.

20. (Previously presented) The method of claim 19, wherein verifying comprises verifying the addresses using an error code correction (ECC) encoder/decoder.

21. (Previously presented) The method of claim 19, wherein verifying the addresses using an error code correction (ECC) encoder/decoder comprises writing encoded data that is stored at the addresses, reading the stored encoded data from the addresses, decoding the encoded data, and identifying any errors in the data.

22. (Previously presented) The method of claim 21, further comprising correcting any errors in the data.

23. (Previously presented) The method of claim 19, wherein the range of addresses comprises a subset of all of the addresses of the data storage device.

24. (Previously presented) The method of claim 19, wherein the range of addresses comprises all of the addresses of the data storage device.

25. (Previously presented) The method of claim 19, further comprising collecting data regarding errors in data stored at one or more of the multiple addresses without interrupting the sequential verifying.

26-27. (Canceled)

28. (Previously presented) The method of claim 19, further comprising terminating the sequential verifying upon an external error occurring.

29. (Previously presented) The method of claim 19, further comprising terminating the sequential verifying upon completion of verifying each address in the range a predetermined number of times.

30. (Previously presented) The method of claim 19, further comprising receiving designation of the start address and the end address.

31. (Currently amended) A memory component, comprising:

a data storage device that includes a plurality of addresses; and

a storage device controller that includes an error correction code (ECC) encoder/decoder and a verify module, the verify module comprising a processor that controls the ECC encoder/decoder to sequentially verify whether or not data stored at addresses of the data storage devices within a range defined by a starting address and an ending address contains an error, ~~and~~ to continuously repeat the sequential verifying of the multiple addresses within the range in a continuous loop such that the verifying can continue indefinitely, and to resume the continuous repeating of the sequential verifying.

32. (Previously presented) The memory component of claim 31, wherein the data storage device is a solid state storage device.

33. (Previously presented) The memory component of claim 31, wherein the data storage device is a magnetic storage device.

34. (Previously presented) The memory component of claim 31, wherein the ECC encoder/decoder is configured to write encoded data that is stored at the addresses, read the stored encoded data from the addresses, decode the encoded data, and identify any errors in the data.

35. (Previously presented) The memory component of claim 34, wherein the ECC encoder/decoder is further configured to correct any errors in the data.

36. (Previously presented) The memory component of claim 31, wherein the verify module further comprises an address counter that stores the starting address.

37. (Previously presented) The memory component of claim 31, wherein the verify module further comprises at least one counter that stores at least one of an indication of the number of times each address within the range is to be verified and the number of data errors that are detected.

38. (Previously presented) The memory component of claim 31, wherein the verify module further comprises a configuration register that stores data used to configure the ECC encoder/decoder.

39. (Previously presented) The memory component of claim 31, wherein the verify module further comprises data transfer hardware that automatically collects data about detected errors without interrupting the processor.

40. (Previously presented) The memory component of claim 31, wherein the range of addresses comprises a subset of all of the addresses of the data storage device.

41. (Previously presented) The memory component of claim 31, wherein the range of addresses comprises all of the addresses of the data storage device.

42. (Previously presented) The memory component of claim 31, wherein the ECC encoder/decoder is further configured to interrupt the sequential verify upon detecting an error in data of one of the addresses.

43. (Canceled)